HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200302164-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Chi-Keung LUK et al.

Confirmation No.: 3236

Application No.: 10/029,699

Examiner: Unknown

Filing Date: 12/18/2001

Group Art Unit: 2183

Title: SOFTWARE CONTROLLED PRE-EXECUTION IN A MULTITHREADING PROCESSOR

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97 (c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: 08/31/2004

OR

( ) I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number _____ on _____
Number of pages:

Typed Name: Colleen F. Brown

Signature: Colleen F. Brown

Respectfully submitted,

Chi-Keung LUK et al.

By _____

Jonathan M. Harris

Attorney/Agent for Applicant(s)
Reg. No. **44,144**

Date: **08/31/2004**

Telephone No.: **(713) 238-8000**

PATENT APPLICATION
Sheet 1 of 1

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
200302164-1	**10/029,699**	**3236**

APPLICANT: **Chi-Keung LUK et al.**

FILING DATE	GROUP
12/18/2001	**2183**

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	5,758,142	05/26/1998	S. McFarling et al.	
	1B	5,933,860	08/03/1999	J. S. Emer et al.	
	1C	6,757,811 B1	06/29/2004	S. S. Mukherjee	
	1D	5,904,732	05/18/1999	D Greenley et al.	
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	
	1R	
	1S	

EXAMINER	DATE CONSIDERED

Please type a plus sign (+) inside this box → [+]

PTO/SB/08B (08-00)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/029,699
Filing Date	12/18/2001
First Named Inventor	Chi-Keung LUK
Group Art Unit	2183
Examiner Name	Unknown
Attorney Docket Number	200302164-1 (1662-46800)

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
	AA	M. Franklin, "Incorporating Fault Tolerance in Superscalar Processors," Proceedings of High Performance Computing, December, 1996 (pp. 301-306).	
	AB	A. Mahmood et al., "Concurrent Error Detection Using Watchdog Processors - A Survey," IEEE Trans. on Computers, Vol. 37, No. 2, February 1988 (pp. 160-174).	
	AC	J. H. Patel et al., "Concurrent Error Detection In ALU's by Recomputing With Shifted Operands," IEEE Trans. on Computers, Vol. 31, No. 7, July 1982 (pp. 589-595).	
	AD	D. A. Reynolds et al., "Fault Detection Capabilities Of Alternating Logic," IEEE Trans. on Computers, Vol. 27, No. 12, December 1978 (pp. 1093-1098).	
	AE	E. Rotenberg et al., "Trace Cache: A Low Latency Approach To High Bandwidth Instruction Fetching," Proceedings of the 29th Annual International Symposium on Microarchitecture, December 1996 (pp. 24-34).	
	AF	E. Rotenberg et al., "Trace Processors," 30th Annual International Symposium on Microarchitecture (MICRO-30), Dec. 1997 (pp. 138-148).	
	AG	T. J. Slegel et al., "IBM's S/390 G5 Microprocessor Design," IEEE Micro, pp. 12-23, March/April 1999 (pp. 12-23).	
	AH	J. E. Smith et al., "Implementing Precise Interrupts In Pipelined Processors," IEEE Trans. on Computers, Vol. 37, No. 5, May 1988 (pp. 562-573).	
	AI	G. S. Sohi et al., "A Study Of Time-Redundant Fault Tolerance Techniques For High-Performance Pipelined Computers," Digest of Papers, 19th International Symposium on Fault-Tolerant Computing, 1989 (pp. 436-443).	
	AJ	G. S. Sohi et al., "Instruction Issue Logic For High-Performance, Interruptible, Multiple Functional Unit, Pipelined Computers," IEEE Transactions on Computers, Vol. 39, No. 3, March 1990 (pp. 349-359).	
	AK	D. M. Tullsen, et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proceedings of the 22nd Annual International Symposium on Computer Architecture, Italy, June 1995 (12 pp.).	
	AL	S. K. Reinhardt et al., "Transient Fault Detection Via Simultaneous Multithreading," undated (12 pp.).	
	AM	L. Spainhower et al., "IBM S/390 Parallel Enterprise Server G5 Fault Tolerance: A Historical Perspective," IBM J. Res. Develop. Vol. 43, No. 5/6, September/November 1999 (pp. 863-873).	
	AN	M. Franklin, "A Study Of Time Redundant Fault Tolerance Techniques For Superscalar Processors," undated (9 pp.).	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.